Remarks

In the Office Action dated November 28, 2005, which was made **FINAL**, ("Final Rejection"), Claims 1-22 were rejected. In the amendment set forth above, Claim 1 is amended and Claim 2 is canceled. The remaining Claims remain as originally presented. It is respectfully requested that the amendment to the Claims be entered for purposes of appeal.

1. The Examiner correctly notes that the reference to serial no. "10/600,218" should be amended to "10/600,205". This change is provided in the amendment to the Specification set forth above.

2. Claim 1 has been amended to include the limitation previously set forth in Claim 2, and Claim 2 has been canceled. Claim 1 is now of a similar scope to the remaining independent Claims. In view of the limitations set forth in independent Claims 9 and 19, and further in view of canceled Claim 2, this amendment should raise no new grounds of rejection. Therefore, it is requested that this amendment be entered for purposes of appeal.

Before considering the language of amended Claim 1 in detail in regards to the current rejection, the language of original Claim 9, which has not been amended, is considered. This Claim was rejected under 35 USC §103(a) as being unpatentable over Applicants' Admitted Prior Art ("AAPA") in view of U.S. Patent No. 6,792,507 to Chiou et al ("Chiou"). This rejection is respectfully traversed.

Claim 9 appears as follows:

9. For use in a system having multiple requesters coupled to a shared memory, a method for controlling processing of requests, comprising:

a.) issuing a request for data by a requester to the shared memory;

b.) providing the data from the shared memory in response to the request before all read-only copies of the data retained by other requesters have been invalidated; and

c.) stalling the requester until all of the read-only copies have been invalidated.

Claim 9 includes the aspect wherein data is provided from a shared memory to a requester *before all read-only copies of the data retained by other requesters have been invalidated*. (Claim 1, step b.) Step c recites stalling the requester until those read-only copies are invalidated. The Examiner cites AAPA page 2 lines 29-30 as teaching Claim 9, step c. (See Final Rejection page 6, last paragraph.) However, the cited passage of the AAPA specifically relates to a prior art system that *does not* provide data *until invalidation operations are complete*, as follows:

> "The read-only copy must generally *be invalidated before a copy of this data is provided to the first IP*....delaying processing activities of the first IP". (AAPA page 2 lines 24-30, emphasis added.)

Thus, the cited AAPA passage cannot possibly teach aspects of the method of Claim 9, which recites a method for "providing the data from the shared memory ... before all read-only copies of the data retained by other requesters have been invalidated". (Claim 9 step b.) To re-state, the AAPA describes invalidating before providing data, whereas Claim 9 describes providing data before invalidating. The AAPA literally, and very specifically, teaches away from

Applicants' invention, and the rejection is therefore improper for at least this reason.

Next, Chiou is considered. The Examiner states that the aspect of Claim 9 related to providing data to a requester before all invalidation operations are complete is taught by Chiou page 15 lines 4-8. The cited passage of Chiou is as follows:

> "In the 'non-critical coherent' mode, data gets written to the target device first, and then the cache gets either updated or invalidated." (Chiou column 15 lines 5-7.)

Two observations may be made regarding the cited passage from Chiou. First, the cited passage of Chiou does not teach Applicants' step b at all for the following reasons. In the Chiou system, storage devices 26 are referred to as "target devices" (see Chiou Figure 1). For instance, storage device 26 at the bottom of Figure 1 is referred to as "Target D". (See also Chiou, column 7 line 32, column 8 lines 33-37, and column 10 line 27.) Host systems 26 can write data to any target storage device by providing a target device address, the device ID, the LUN ID, some additional addressing information, and the data. (See, for example, column 9 line 4-6.) The write operation can occur either in a critical coherent mode wherein the intervening caches get updated or invalidated before the data gets written to the target device. Alternatively, In a non-critical coherent mode, data gets written to the target device first, and then the cache gets updated or invalidated, as described in the Chiou passage cited by the Examiner.

In contrast to the Chiou system, Applicants' Claim 9 describes

a.) issuing a request for data by a requester to the shared memory; and

b.) providing the data from the shared memory in response to the request before all read-only copies of the data retained by other requesters have been invalidated.

In other words, Claim 9 describes a read scenario wherein a requester (such as an instruction processor) is requesting data from memory, and in response, the memory provides the data to the requester before invalidation operations are completed.

It appears from the cited Chiou passage that the Examiner is equating the Chiou target device with Applicants' requester of Claim 9, since it is the Chiou target device that is receiving the data. However, the Chiou target storage device did not issue a request for data to the shared memory as claimed by Applicants' step a.). Instead, Chiou is discussing an entirely different type of scenario wherein data is being *written* to the target storage device upon the issuance of a write request from a host such as host A 26 (Chiou Figure 1). To re-state, Chiou does not teach a requester that requests data from a shared memory, and a shared memory that then provides the data to the request as recited by steps a and b of Applicants' Claim 9. For at least this reason, Chiou is entirely related to Applicants' invention of Claim 9, and does not teach or suggest any aspect of Applicants' Claim 9. The Examiner is attempting to isolate unrelated portions of the description from each reference and piece them together to teach Applicants' invention in a manner that is improper. For at least this reason, this rejection is improper, and should be withdrawn.

In addition to the foregoing, the cited passage of Chiou very clearly states that any invalidation operations occur after data is provided to the requester. In contrast, the AAPA passage cited by the Examiner and quoted above specifically relates to a method for completing invalidation operations before data is provided to the requester. The method of Chiou and the method described in the AAPA are mutually exclusive, and teachings from the AAPA cannot properly be

combined with teachings from Chiou for this reason. For at least this reason, this rejection is improper.

Next, Claims 10-18 are considered. These Claims are rejected on the same basis as Claim 9. (See Final Rejection page 6.) These Claims depend from Claim 9, and are allowable for at least the reasons set forth above in regards to Claim 9. These Claims further include other scopes and aspects not taught by the prior art, and are allowable for the additional reasons discussed in the response filed October 13, 2005. For example, Claim 10 includes initiation of a hardware sequence to stall the requester in step c. Claim 11 describes execution of an instruction to initiate the hardware sequence. Claim 12 describes the instruction as being part of the hardware instruction set of an instruction processor. These additional aspects are not taught or suggested by the cited combination of references, and for these additional reasons, these Claims are allowable over this rejection.

Turning next to Claim 19, this Claim, which remains as originally presented, is rejected under 35 USC §102(a) based on the AAPA. (See Final Rejection page 2.) This Claim includes aspects similar to those set forth in regards to Claim 14, including the aspect wherein data is provided in response to a request before all read-only copies of the data have been invalidated. Therefore, it will be assumed for further discussion purposes that the Examiner intended to reject this Claim under 35 USC §103(a) based on AAPA and Chiou. *If this is an incorrect assumption, further clarification is requested.*

Claim 19 describes issuing a request for data by a processor to a shared memory, providing the data to the processor before all invalidation operations have occurred for this data, and then stalling the processor until all of the read-only copies have been invalidated. For at least the reasons discussed above, the rejection based on the AAPA and Chiou does not teach or suggest this method. Moreover, the rejection is improper since the cited passage of the

AAPA very specifically teaches away from Applicants' invention and from the cited passage of Chiou.

Claims 15 – 22 depend from Claim 14 and are allowable for at least the reasons discussed in regards to Claim 14. These Claims include additional aspects not taught by the cited combination of references. For example, Claim 16 describes stalling a processor until all read-only copies of *any data* (not just the requested data) that has been provided to that processor have been invalidated. Claim 17 describes stalling a processor until all read-only copies of *any data* previously provided to *a predetermined set of processors* in the system have been invalidated. Claim 18 describes issuing an inter-processor interrupt to another requester to indicate that data may be accessed by that other requester. Claim 22 describes request tracking means for delaying return of data to a requester until all read-only copies of other data that has been previously requested by that processor have been invalidated. None of these aspects are taught by the cited combination of references. For these additional reasons, these Claims are allowable over the current rejection.

Next, Claim 1 is again considered. Claims 1 was rejected under 35 USC §102(a) as being anticipated by pages 1-3 of Applicants' Admitted Prior Art ("AAPA"). This rejection is respectfully traversed.

As amended, Claim 1 includes the aspect of previously presented Claim 2, which has been canceled. Amended Claim 1 includes aspects that are similar to Claims 9 and 14 discussed above. This Claim is therefore allowable for the reasons discussed above in regards to Claims 9 and 14.

Claim 1 further describes a circuit to execute an instruction to cause the first requester to temporarily enter a stalled state. It may be noted that while the passage of the AAPA cited by the Examiner as teaching this aspect of Claim 1 describes the general delaying of processing activities, this AAPA passage does not mention any circuit to execute an instruction to cause the requester to temporarily enter a stalled state. Since there are many ways processing

activities can be delayed (e.g., in software), this generalized reference in the AAPA to delayed processing activities does not teach this additional aspect of Claim 1. For this additional reason, Claim 1 is allowable over this rejection.

Claims 3-8 are allowable over this rejection for at least the reasons discussed above in regards to Claim 1. Moreover, these Claims include additional aspects not taught by any of the cited references. For example, Claim 3 describes a memory circuit for providing data before invalidation operations are completed, wherein the circuit includes both a request and response channel. Claim 4 further describes an acknowledge tracker. Claim 5 describes a request tracking circuit. Claims 6-8 describe aspects related to a first requester that issues multiple requests, and wherein the circuit of Claim 1 prevents processing from occurring until *all* invalidation operation for *all* requests have been completed. None of these aspects are taught or suggested by the cited combination of references. For at least these additional reasons, these Claims are allowable over the current rejection.

3. The prior art made of record and not relied upon has been reviewed and is considered to be of general interest only.

Conclusion

In the Office Action dated November 28, 2005, which was made Final, Claims 1-22 were rejected. In the Amendment set forth above, Claim 1 is amended, Claim 2 is canceled, and the remaining Claims are unchanged. In view of the amendments to the Claims and the comments set forth above, it is respectfully submitted that all Claims are allowable over the cited prior art, and are in condition for allowance as presently presented. Therefore, a Notice of Allowance is respectfully requested. If a Notice of Allowance is not issued, it is respectfully requested the amendments to the Claims be entered for purposes of appeal, as these amendments do not raise new grounds for rejection. If the Examiner has questions or comments regarding any of the foregoing, a call to the undersigned is encouraged and welcomed.

Respectfully submitted,

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